

Design of MOS-translinear Multiplier/Dividers in Analog VLSI

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A general framework for designing current-mode CMOS analog multiplier/divider circuits based on the cascade connection of a geometric-mean circuit and a squarer/divider is presented. It is shown how both building blocks can be readily obtained from a generic second-order MOS translinear loop. Various implementations are proposed, featuring simplicity, favorable precision and wide dynamic range. They can be successfully employed in a wide range of analog VLSI processing tasks. Experimental results of two versions, based on stacked and folded MOS-translinear loops and fabricated in a 2.4- μm CMOS process, are provided in order to verify the correctness of the proposed approach.

Keywords: Analog multiplier/dividers; Multipliers; MOS-translinear; Voltage-translinear; CMOS analog circuits; Analog VLSI

1. INTRODUCTION

The area of analog multipliers constitutes a field of active research due to their wide applicability in analog signal processing. Frequency translation, phase detection, correlation, convolution, adaptive filtering, *etc.*, are usually achieved using these circuits; moreover, novel applications are steadily increasing this already extensive list, *e.g.*, Square-Root Domain companding systems [1].

Nevertheless, most of existing proposals are designed for voltage-mode applications, and the availability of general-purpose current multipliers in CMOS technology is still modest [2].

Some CMOS solutions have been proposed either using transistors in the linear region (*e.g.* [3]), or in the saturation region often employing the quarter-square identity (*e.g.* [4]). The use of the translinear principle in MOS transistors operating in strong inversion and saturation

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(MOS-translinear principle [5]) has also been proposed in [6] for this purpose, though the complexity involved in the design seems unnecessary.

In this paper, a novel approach for designing current-mode analog multiplier/divider circuits is presented, based on the cascade connection of a geometric-mean circuit and a squarer/divider circuit. The resulting topology is very well suited for being fully implemented in standard CMOS using MOS-translinear (MTL) loops, as will be evidenced subsequently. It can be successfully applied to a wide range of different analog systems, featuring simplicity, favorable precision, an area-efficient implementation due to the fact that only MOS transistors are employed, and wide dynamic range originated from the current-mode approach followed. In addition, insensitivity to temperature and process variations is inherited from its MOS-translinear nature.

2. BASIC PRINCIPLE

A simple procedure for obtaining a current multiplier/divider is to generate a current which is the geometric-mean of two currents I_x and I_y , i.e.,

$$I_{gm} = k\sqrt{I_x I_y} \quad (1)$$

being k a nonzero arbitrary constant; if this current is injected into a squarer/divider circuit having the following input–output characteristic:

$$I_{out} = \frac{I_{in}^2}{k^2 I_w} \quad (2)$$

then the squarer/divider output will be given by the expression

$$I_{out} = \frac{\left(k\sqrt{I_x I_y}\right)^2}{k^2 I_w} \quad (3)$$

that can be equivalently written as

$$I_{out} = \frac{I_x I_y}{I_w} \quad (4)$$

Hence, according to (4), a current-mode multiplier/divider could be obtained by this simple method. This idea is shown in Figure 1.

Since Eqs. (1) and (2) are inverse one each other, it can be expected that both could be implemented in practice using the same basic topology, by just interchanging input by output and properly adapting the input and output impedances. A general approach to the design of the required blocks using MOS-translinear techniques will be provided in the next section.

3. MULTIPLIER/DIVIDER DESIGN

Both squarer/divider and geometric-mean cells can be obtained by using either the stacked or folded second-order MTL loops shown in Figures 2a and 2b, respectively. In both cases, applying the KVL to the loop and assuming MOS transistors operating in saturation and having equal transconductance factors and threshold voltages, the

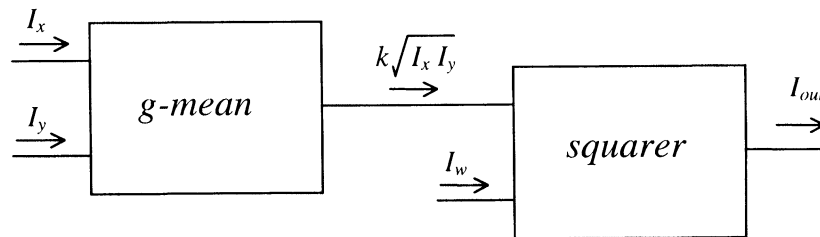


FIGURE 1 Principle of the multiplier/divider circuit.

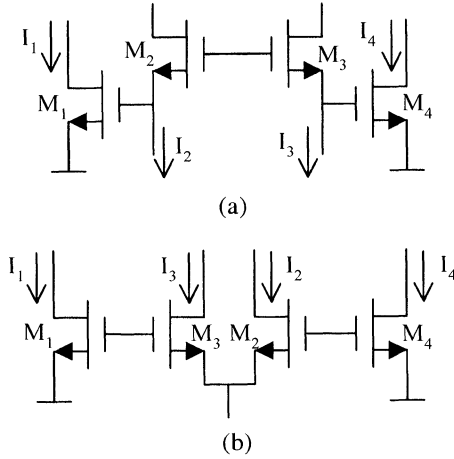


FIGURE 2 MOS-translinear loop (a) Stacked topology (b) Folded topology.

following expression is obtained:

$$\begin{aligned} \sqrt{\frac{I_1}{(W_1/L_1)}} + \sqrt{\frac{I_2}{(W_2/L_2)}} \\ = \sqrt{\frac{I_3}{(W_3/L_3)}} + \sqrt{\frac{I_4}{(W_4/L_4)}} \end{aligned} \quad (5)$$

being I_i and W_i/L_i the drain current and aspect ratio, respectively, of transistor M_i ($i = 1, 2, 3, 4$).

The folded topology has some important advantages, not the least of them being the possibility of decreasing the supply voltage requirements (if a proper biasing is applied), and alleviating the V_{TH} mismatch due to the bulk effect that adversely affects the stacked topology if technology precludes the connection of MOST source terminals to their bulk terminals (*i.e.*, NMOS loops in n -well technology).

If the following aspect ratios are chosen

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = k^2 \frac{W_1}{L_1} = k^2 \frac{W_2}{L_2} \quad (6)$$

being k a positive constant, and the strategy for injecting currents into the MTL loop is such that

$$I_3 = I_4 = \frac{k^2(I_1 + I_2) + 2kI_5}{4} \quad (7)$$

for a certain current I_5 , the following relationship among I_1 , I_2 and I_5 is revealed after squaring both sides in (5) and rearranging,

$$I_5 = k\sqrt{I_1 I_2} \quad (8)$$

Therefore, a geometric-mean circuit is obtained if I_1 and I_2 are the input currents and the output current is a copy of I_5 . Alternatively, a squarer/divider is obtained if the output is a copy of either I_1 or I_2 and the inputs are the remaining two currents, being, respectively,

$$I_1 = \frac{I_5^2}{k^2 I_2} \quad \text{or} \quad I_2 = \frac{I_5^2}{k^2 I_1} \quad (9)$$

Table I illustrates four possible designs which result from combining the two proposed kinds of MOS translinear loops, and two values for the k parameter previously introduced. A number of different practical circuits result by using different values for k , and by implementing alternative schemes for current injection into the four-transistor MOS-translinear loops. Also, PMOS and/or NMOS loops can be used depending on the available technology. Note that the choice of the current injection strategy is far from trivial, since it has a strong influence in the area occupied, power consumption and potential for low-voltage operation. Some of the multiplier/dividers achievable, according to the schemes in Table I, will be presented subsequently.

3.1. Stacked MTL Loop; $k = 2$

Using the blocks shown in the first row of Table I in the diagram of Figure 1, a version of the multiplier/divider is constructed; the detailed schematic of the circuit thus obtained is shown in Figure 3. The MOS-translinear loops of the geometric-mean and squarer/divider circuits are formed by (PMOS) transistors $M_{1A}-M_{4A}$ and $M_{1B}-M_{4B}$, respectively; the bulk terminals of these transistors are connected to their sources, thus avoiding the bulk effect. Note that the relative aspect ratio of these transistors is determined by

TABLE I Some possible building blocks for the multiplier/divider

	Geometric Mean, $I_{out} = k\sqrt{I_1 I_2}$	Squarer/Divider, $I_{out} = I_5^2/k^2 I_{1,2}$
Stacked		
$k=2$		
Folded		
$k=1$		

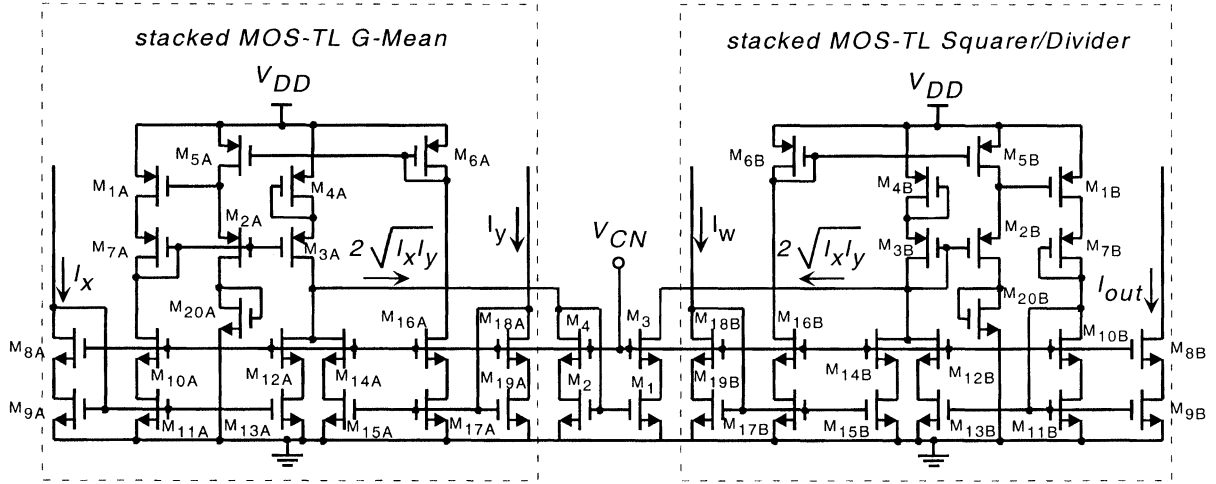


FIGURE 3 Multiplier/divider using stacked MTL loops.

the choice for k employed, according to (6). M_{7A-B} and M_{20A-B} are diode-connected transistors included for alleviating the channel-length modulation effect in M_{1A-B} and M_{2A-B} , respectively. Transistors M_{5A-B} – M_{6A-B} form simple current mirrors, and M_{8A-B} – M_{19A-B} constitute high-swing cascode current copiers employed for injecting the required combinations of currents into the MOS-translinear loops. The middle current mirror formed by transistors M_1 – M_4 is employed for inverting the output current of the geometric-mean block in order to be properly introduced into the squarer/divider. Note the similarity of the geometric-mean and squarer/divider

blocks employed, which is beneficial in terms of matching between both blocks, thus improving the multiplier/divider performance.

3.2. Folded MTL Loop; $k=1$

As mentioned elsewhere, the stacked topology of Figure 2a suffers from the bulk effect if technology does not allow an independent connection of the bulk terminals; this can seriously affect the loop behavior. This shortcoming is greatly alleviated using the folded MOS-translinear loops shown in the second row of Table II as the required blocks of the multiplier/divider. A possible way of

TABLE II Transistor aspect ratios in the circuit of Figure 3*

	M_{1A-2A}	M_{3A-4A}	M_{5A-6A}	M_{7A}	M_{8A-19A}	M_{20A}	M_{1-4}
L (μm)	9.6	9.6	9.6	2.4	5.6	2.4	5.6
W (μm)	80	320	160	80	100	96	56

*Transistors $M_{iB} = M_{iA}$ for all i .

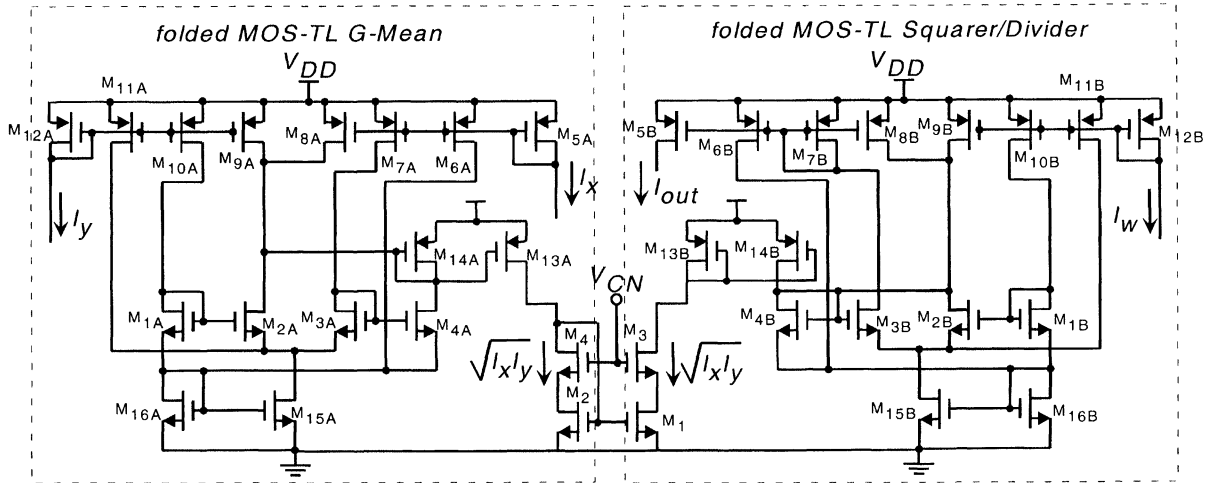


FIGURE 4 Multiplier/divider using folded MTL loops.

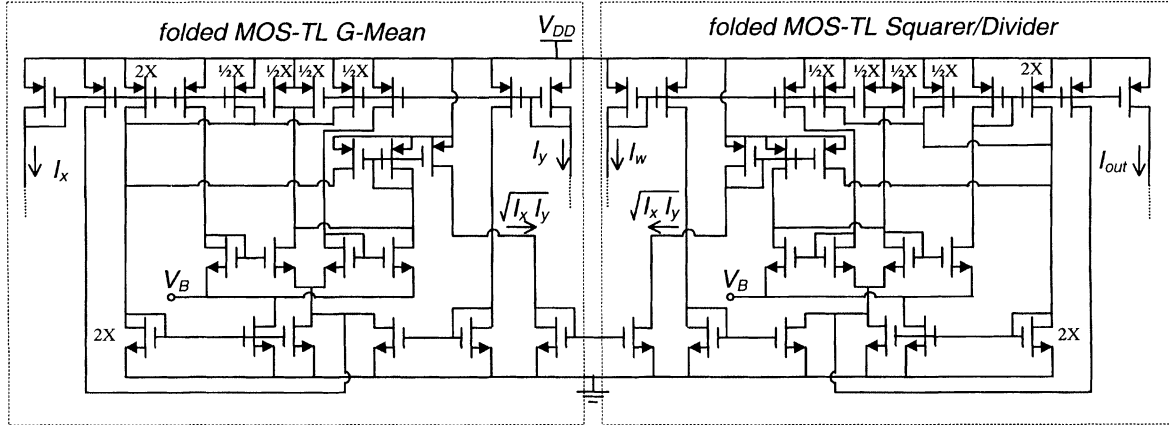


FIGURE 5 Multiplier/divider using folded MTL loops, low-voltage alternative.

injecting the loop currents is shown in the circuit of Figure 4. The folded MOS-translinear loops are formed by transistors $M_{1A}-M_{4A}$ and $M_{1B}-M_{4B}$; since $k=1$ in (6), the loop transistors are equally sized. The remaining transistors constitute current copiers that inject the appropriate loop currents.

A similar voltage supply than the stacked topology is required, due to the stacking of diode-connected transistors employed, thus not fully exploiting its low-voltage capability. An alternative way of injecting the loop currents is shown in the multiplier/divider of Figure 5, allowing to

operate at a supply voltage as low as one V_{GS} plus two V_{DS} of a saturated MOST. This is achieved by avoiding diode-connected transistors at the sources of the loop transistors (shaded areas). V_B keeps the biasing transistors at the bottom in saturation for any input currents.

4. SIMULATION AND MEASUREMENT RESULTS

The multiplier/dividers of Figures 3 and 4 were fabricated on a monolithic IC using a n -well 2.4- μm CMOS process. The circuit of Figure 3 was firstly tested. The aspect ratios chosen are shown in Table II. Supply voltage was $V_{DD}=5\text{ V}$, and $V_{CN}=2.3\text{ V}$. Figure 6 shows the measured multiplier/divider DC characteristics obtained for $I_w=10\text{ }\mu\text{A}$, I_y values ranging from $0\text{ }\mu\text{A}$ (lower

line) to $10\text{ }\mu\text{A}$ (upper line) in $2.5\text{ }\mu\text{A}$ steps and I_x swept from 0 to $100\text{ }\mu\text{A}$. The good linearity obtained is readily noticeable.

The measured output THD at 10 kHz , for an input sinusoid with DC component $I_{DC}=50\text{ }\mu\text{A}$, was well below 2% for input peak amplitudes as large as $45\text{ }\mu\text{A}$. I_y and I_w were set to $10\text{ }\mu\text{A}$ for this measurement.

Subsequently, the circuit of Figure 4 was tested. The aspect ratios chosen are offered in Table III. When compared to the circuit of Figure 3, a certain loss in dynamic range is observed since a 3.3 V supply was employed; V_{CN} was set to 1.5 V . Figure 7 shows a microphotograph of the circuit; the area occupied is 0.19 mm^2 . In Figure 8, the measured DC characteristics are shown; I_w was kept to a constant value of $15\text{ }\mu\text{A}$, whereas I_x was stepped from $15\text{ }\mu\text{A}$ to $40\text{ }\mu\text{A}$ in $5\text{ }\mu\text{A}$ steps and I_y was swept from 0 to $25\text{ }\mu\text{A}$. The measured THD at

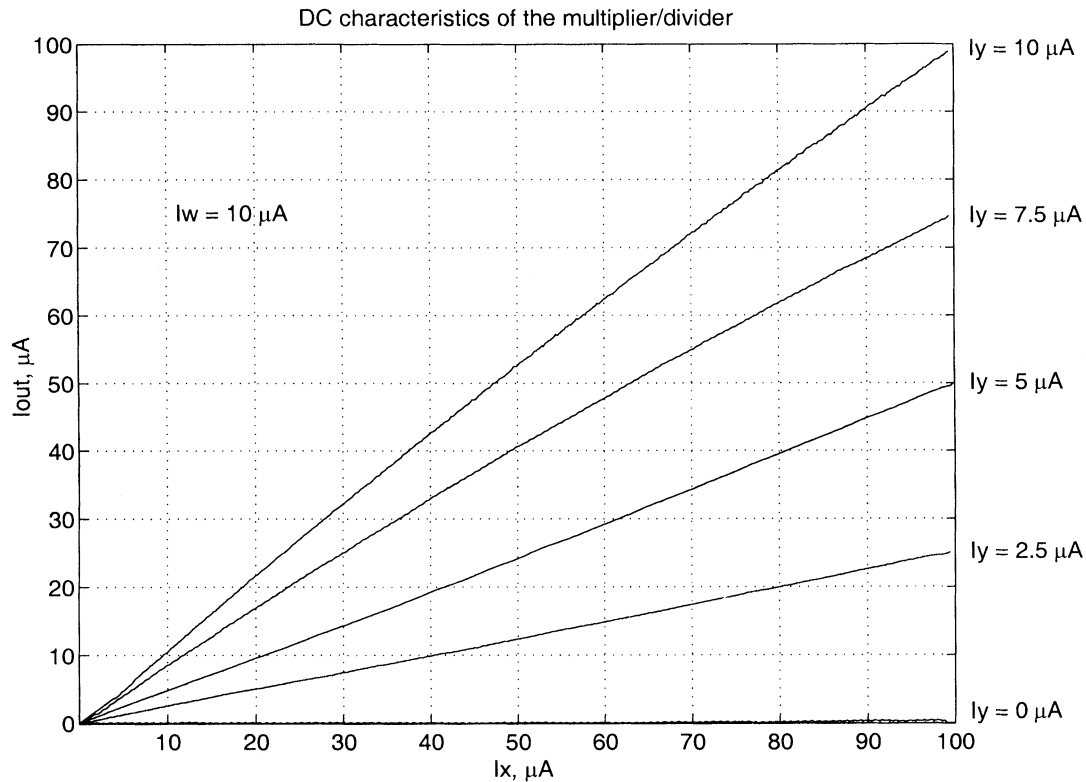


FIGURE 6 Measured DC transfer characteristics of the multiplier/divider of Figure 3 for different bias currents.

TABLE III Transistor aspect ratios in the circuit of Figure 4*

	M_{1A-4A}	M_{5A-7A}	M_{8A-9A}	$M_{10A-14A}$	$M_{15A-16A}$	M_{1-4}
L (μm)	12	7.2	7.2	7.2	5.6	5.6
W (μm)	80	336	168	336	177.6	56

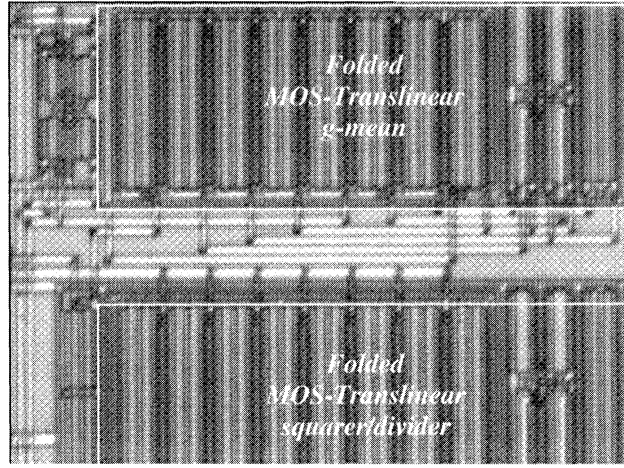
* Transistors $M_{iB} = M_{iA}$ for all i .

FIGURE 7 Microphotograph of the circuit of Figure 4.

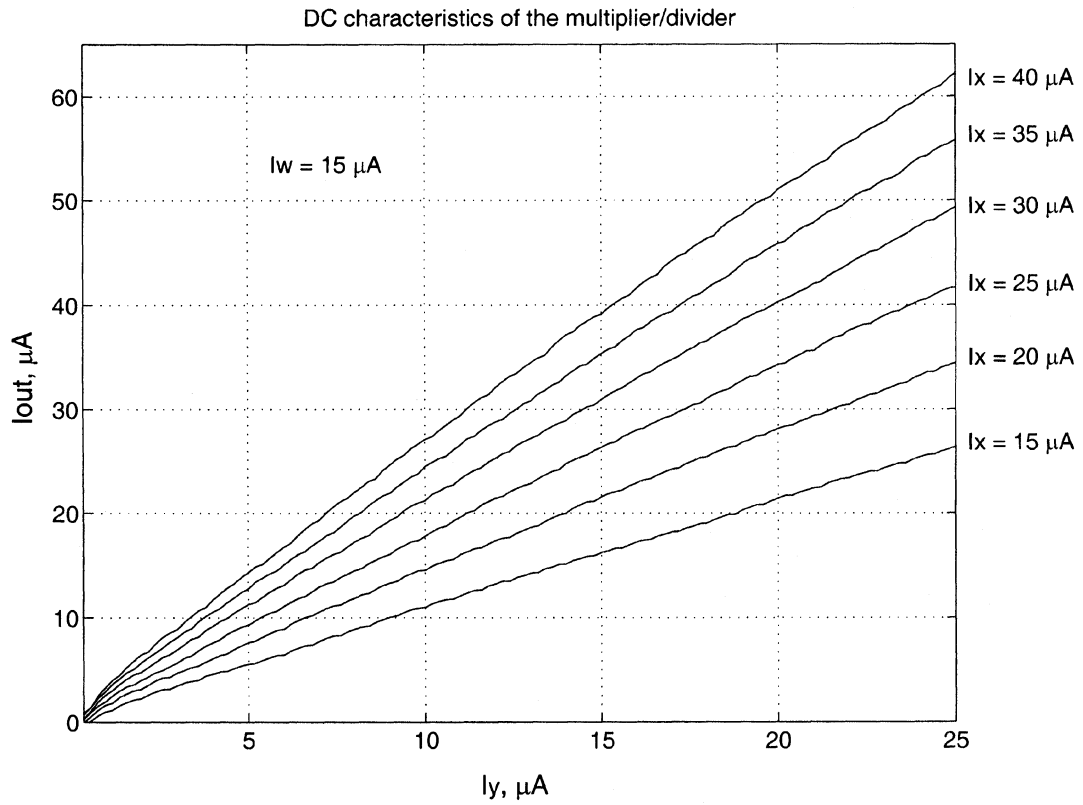


FIGURE 8 Measured DC transfer characteristics of the multiplier/divider of Figure 4 for different bias currents.

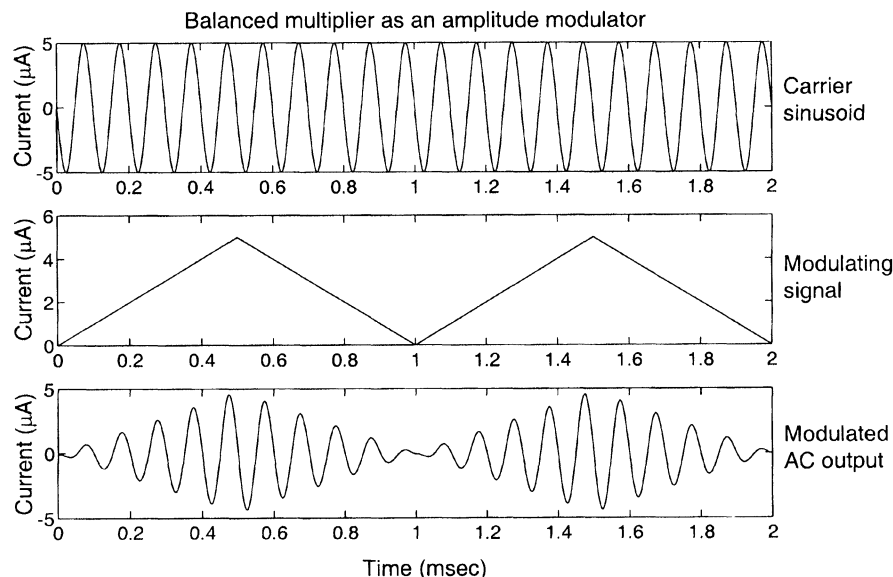


FIGURE 9 Balanced multiplier as an amplitude modulator. 10 kHz carrier sinusoid (upper waveform); 1 kHz modulating signal (middle waveform); AC modulated output (lower waveform).

10 kHz is less than 2% for input sinusoids having peak amplitudes as large as $10\ \mu\text{A}$, and a $11\ \mu\text{A}$ DC component.

A four-quadrant multiplier can be readily obtained from the above multiplier/divider circuits by using a couple of them in a balanced structure. This configuration was only simulated due to the lack of two separate multiplier/dividers on the same chip; the multiplier/divider shown in Figure 5 was employed for these simulations. A 1.5 V operation could be obtained using models from a $0.7\text{-}\mu\text{m}$ CMOS process; the basic aspect ratios employed were (30/4) and (60/4) for the NMOS and PMOS transistors, respectively. Figure 9 shows how such balanced version can be employed as an amplitude modulator. I_x was $10(1 + 0.5\sin(2\pi ft))\ \mu\text{A}$, with $f = 10\ \text{kHz}$, whereas I_y was the modulating waveform, corresponding to a triangular periodic wave; I_w was set to $10\ \mu\text{A}$.

5. CONCLUSIONS

A novel approach to the design of analog multiplier/divider circuits has been presented, which is

based on the cascade connection of a geometric-mean block and a squarer/divider obtained using essentially the same cell (a simple second-order MOS-translinear loop). Measurement results of two versions of the circuit have been offered, confirming in practice the feasibility of this approach. The precision and simplicity of the resulting topologies make them suitable for being applied in a varied repertory of analog VLSI circuitry, in areas such as analog neural computation and analog fuzzy hardware. The performance of the multiplier/dividers proposed here is quite similar in terms of linearity and dynamic range to other proposals based on the MOS-translinear principle, *e.g.* [6]. Nevertheless, the circuits proposed here employ just a couple of MOS-translinear loops, whereas in [6] three loops are required, thus unnecessarily complicating the design and leading to an increase in power and area consumption.

Acknowledgments

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Authors' Biographies

Antonio J. Lopez-martin obtained its M.Sc. and Ph.D. degrees from the Public University of Navarra, Pamplona (Spain) in 1995 and 1999, respectively. He has been at the New Mexico State University, Las Cruces, and the Swiss Federal Institute of Technology, Zürich, as an invited

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Alfonso Carlosena was born in Navarra (Spain) in 1962. He received the M.Sc. degree with honors and the Ph.D. in physics in 1985 and 1989, respectively from the University of Zaragoza, Spain. From 1986 to 1992 he was Assistant Teacher in the Department of Electrical Engineering and Computer Science of the University of Zaragoza. From October, 1992, he has been an Associate Professor at the Public University of Navarra, where he has also served as Head of the Technology Transfer Office. He has also visited other Universities such as the Swiss Federal Institute of Technology (Zurich) and the New Mexico State University. His research interests are in the areas of classical circuit theory, analog circuits and signal processing, digital signal processing and instrumentation, where he has published about fifty papers in international journals and a similar number of conference presentations.

